Deliverable Report

Deliverable No: D2.2

Deliverable Title: Architecture for silicon nitride platform

Grant Agreement number: 899544

Project acronym: PHOQUSING

Project title: PHOtonic Quantum SamplING machine

Project website address: www.phoqusing.eu

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Deliverable table

Deliverable no.	D2.2
Deliverable name	Architecture for silicon nitride platform
WP no.	2
Lead beneficiary	UNIROMA1
Type	Report
Dissemination level	Public
Delivery date from Annex I	M18
Actual delivery date	28 February 2022

What was planned *(from Annex I:)*

D2.2: Architecture for silicon nitride platform [18]
Report on the definition of the most appropriate architecture for integrated circuits based on the silicon nitride platform, for manipulation of multiphoton states. Peculiar properties of the fabrication technique, which enables a large number of integrated passive and active elements, will be included in the analysis.

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HORIZON 2020

What was done

In integrated photonics the silicon nitride platform is to date one of the promising platforms to achieve efficient quantum photonic devices due to its maturity and inherent low losses. In Deliverable 2.2, we have analysed the architecture for the silicon nitride platform for the use with GaAs-based single photon sources which operate at a wavelength of 925nm. While for common wavelengths such as the telecommunication O- and C -band, at 1300nm and 1550nm, respectively, standard building blocks are commonly available, this is not the case for the wavelength of 925nm. Here, we calculated the optimal architecture for this wavelength to achieve both compact and efficient devices at minimum losses which are needed for quantum photonic applications.

Architecture

The most general (linear optics) transformation one can do on N optical modes is an arbitrary $N \times N$ unitary operation U. If one could reliably and quickly generate that operation on-chip, then all bespoke chips or devices for N or fewer modes is entirely redundant.

Fortunately, doing so is entirely possible: Reck et al. showed that there is an efficient mapping from the elements of U to the values of phase shifters and beamsplitters [Reck1994]. This "Reck decomposition" was used in experiments for many years, both in bulk optics and on-chip: it was well known and relatively easy to implement, requiring the minimum number (N^2) of optical elements to represent U. However, as it often turns out, the very first method published on a topic is rarely the optimal one, and the Reck decomposition has several major flaws: it is asymmetric with respect to the optical depth of the circuit, with some of the paths from input to output traversing up to $2N$ elements and some only 1 element. As no such network is free of loss, this path length difference leads to systematic errors in the implementation of U in practice, as well as increased loss in on-chip implementations.

An optimal decomposition is instead symmetric with respect to the input modes. Clements et al. showed one such decomposition several years ago, which requires a square lattice of tunable beamsplitters with a phase shifter on one arm of each beamsplitter's input [Clements2016]. Again, the "Clements decomposition" can be efficiently found from any matrix U. For operational reasons, a related decomposition is used in our chips with the phase shifters *after* the beamsplitters, which improves characterization in practice. It should be noted that, on-chip, each of the tunable beamsplitters is implemented by using two directional 3-dB couplers with a phase shifter between them, forming a tunable Mach-Zehnder interferometer. This represents the current state-of-the-art devices of QuiX Quantum, presenting world-record size and low-loss, based on the silicon-nide TriPleX technology, while being able to implement arbitrary N-mode operations for up to 12 modes (including multiple parallel operations on fewer modes) at an operating wavelength around 1550nm [Roeloffzen2018, Taballione2021]. An advanced version with up to 20 modes will be released in March 2022 with the corresponding scientific publication being prepared at the moment.

However, there are further improvements that can be included. In practice, the phase shifters inside and outside the tunable beamsplitters represent most of the length of the chip, and at each step of the Clements (or QuiX) decompositions only half of the waveguides have a phase shifter present. Bell and Walmsley, building on earlier work, pointed out that instead all of the phase-shifters can be moved inside the tunable beamsplitters, with one phase shifter on each arm of the Mach-Zehnder interferometer as well as on the "edges" of the mesh [Bell2021]. This reduces the total optical length of the circuit by a factor of about 1/3, reducing loss commensurately, while still being efficiently calculable. Moreover, the Bell decomposition is robust against fabrication defects, containing one redundant heater per column.

To further scale up the number of modes for future designs, it is worth investigating a shift from the current QuiX decomposition to the one suggested by Bell2021. While this will require developing new control systems and characterization techniques, the improvement in optical loss and compactness is valuable technically, and therefore in improved scientific outputs.

For PhoQusing, the main challenge of the first series of photonic integrated circuits is to transfer the knowledge and performance of the silicon nitride platform from the common telecom wavelength of 1550nm to 925nm, the operating wavelength of high-performance single photon emitters based on GaAs quantum dots. To minimize the risk, we chose to use the QuiX decomposition as it has already a well-tested performance.

Device geometry

To transfer the architectures as mentioned above, the basic building blocks need to be redesigned in order to fit the targeted wavelength of 925nm. The basic building blocks for any of the above-mentioned architectures are waveguide bends, direction couplers and spot-size converters. For PhoQusing, QuiX Quantum chose, in close discussion with the foundry LioniX International, to go for a symmetric double stripe as it was expected from experience that this would give the best performance in terms for propagation losses and bending radius. A schematic of the cross-section of a symmetric double stripe geometry is shown in Figure 1. The geometry consists of two symmetric stripes of silicon nitride (SiN) surrounded by a silicon dioxide (silica, SiO_2) cladding. Both stripes have a width, *w*, and a thickness, *t*, and are horizontally separated by a gap, *g*. For fabrication reason, we chose a gap of 250nm.

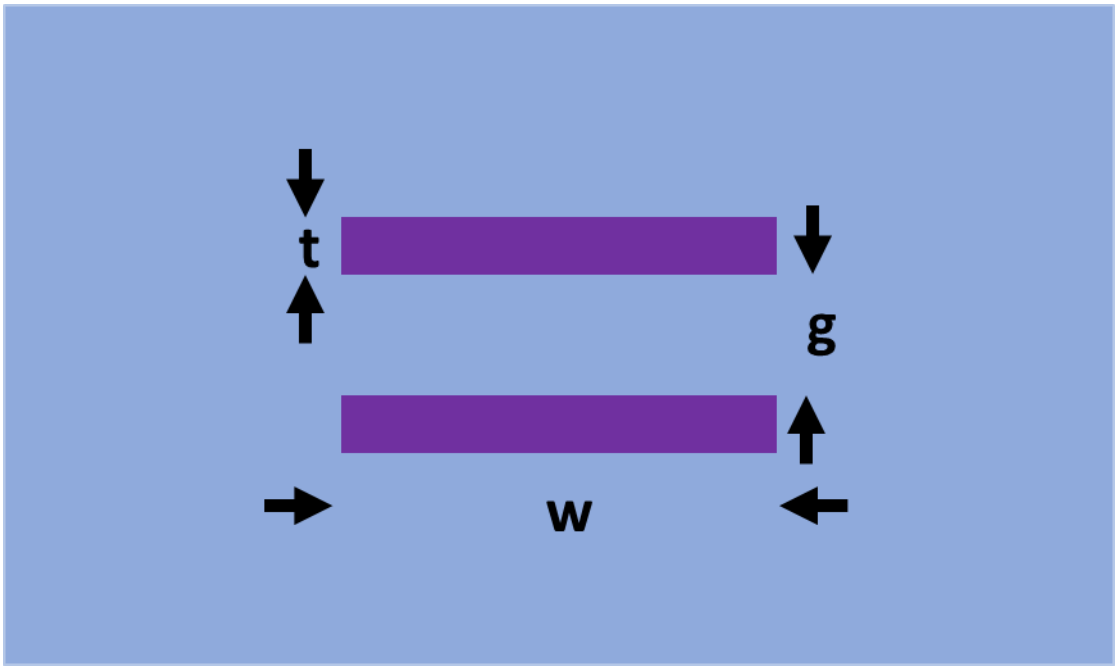

Figure 1: Schematic of the symmetric double stripe geometry comprising two stripes of SiN in a silica cladding. The SiN stripes both have a thickness, t, and a width, w, and are horizontally separated by a gap, g.

The first parameter that was studied to optimize the waveguide cross-section was the thickness of the two SiN stripes. Here, single-mode waveguide width as a function of thickness, t, was simulated. The results are shown in Figure 2 and give the maximum waveguide width that should be used in a design for a given *t* in order to preserve single-mode operation, which is important for the performance of the devices.

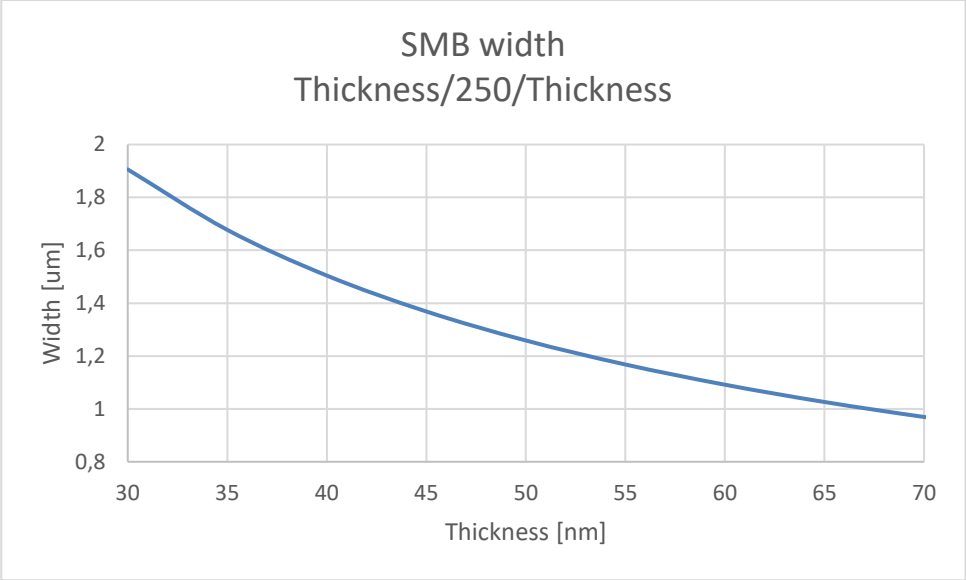

Figure 2: Single-mode waveguide width of the symmetric double stripe at a wavelength of 925nm as a function of stripe thickness.

Based on the resulting waveguide widths shown in Figure 2, the minimum bending radius that can be achieved is calculated. We set our maximum allowable bending radius for PhoQusing to be 200µm since we calculated that this is the maximum bending radius allowed in order to fit a 20 mode processor using the QuiX decomposition onto a single reticle for the lithography. The results of the minimum bending radius are shown in Figure 3.

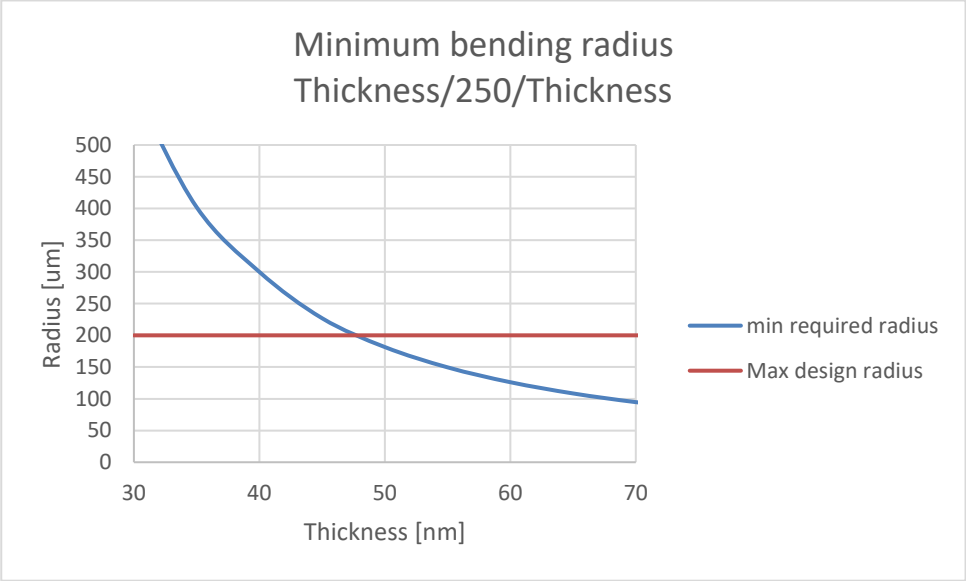

Figure 3: Minimum bending radius as a function of thickness, t. The maximum bending radius is chosen to fit a 20-mode processor in a single reticle.

As can be seen in Figure 3 the minimum thickness should be above 45 nm to fit the design onto a single reticle.

The next building block that was analysed were the 3-dB directional couplers. The fabrication precision of the directional couplers is crucial for the performance of the real-world devices as it can limit how good certain transformation can be performed using the processor. We simulated the maximum error based on the fabrication uncertainties as a function of thickness, t. The results are shown in Figure 4.

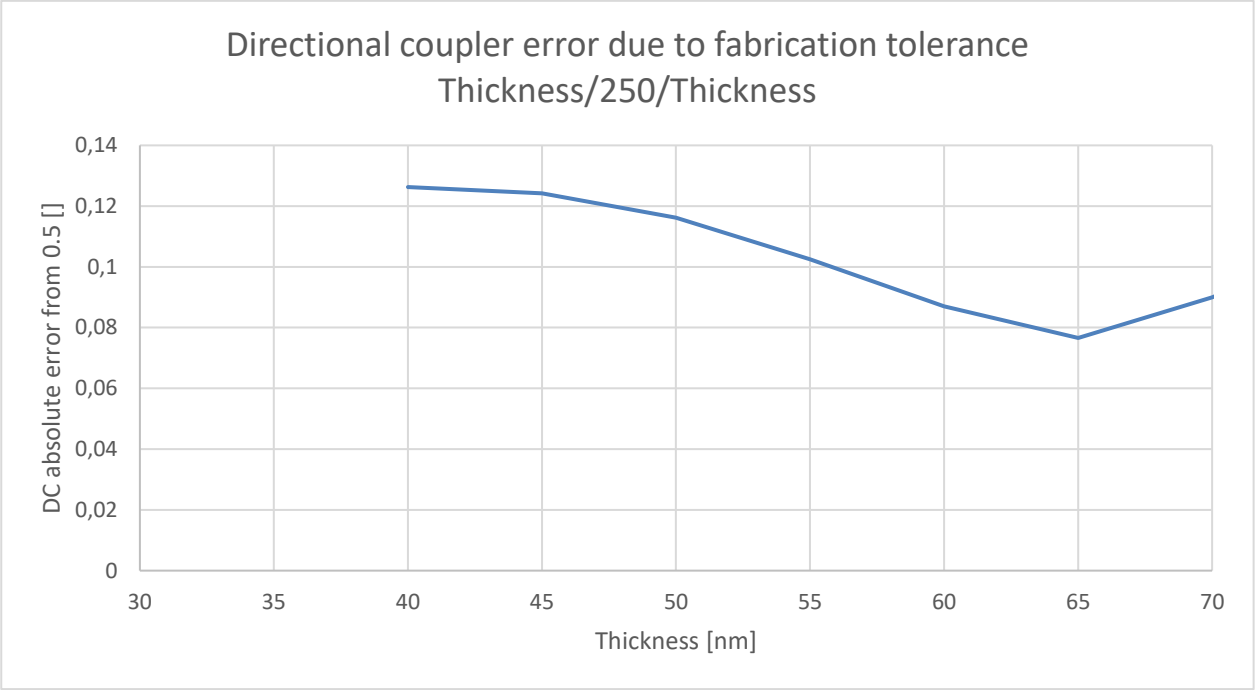

Figure 4: Maximum error of the directional couplers with respect to fabrication tolerances as a function of thickness, t.

As can be seen in Figure 4, we found a minimum worst-case error for the directional couplers to be at a thickness of 65nm. This thickness also results in an acceptable bending radius of 110µm at a waveguide width of 1.0 µm. Consequently, we chose to use the following parameters for the PhoQusing design: t = 65 nm, w=1.0 µm.

The last building block that is crucial for the performance of the processor is the spot-size converter. The spot-size converter is important to allow for efficient coupling from fiber to chip. To calculate the fiber-chip coupling at 925nm, we calculated the mode overlap of the waveguide mode with the mode of a optical fiber (type 780HP). The results are shown in Figure 5.

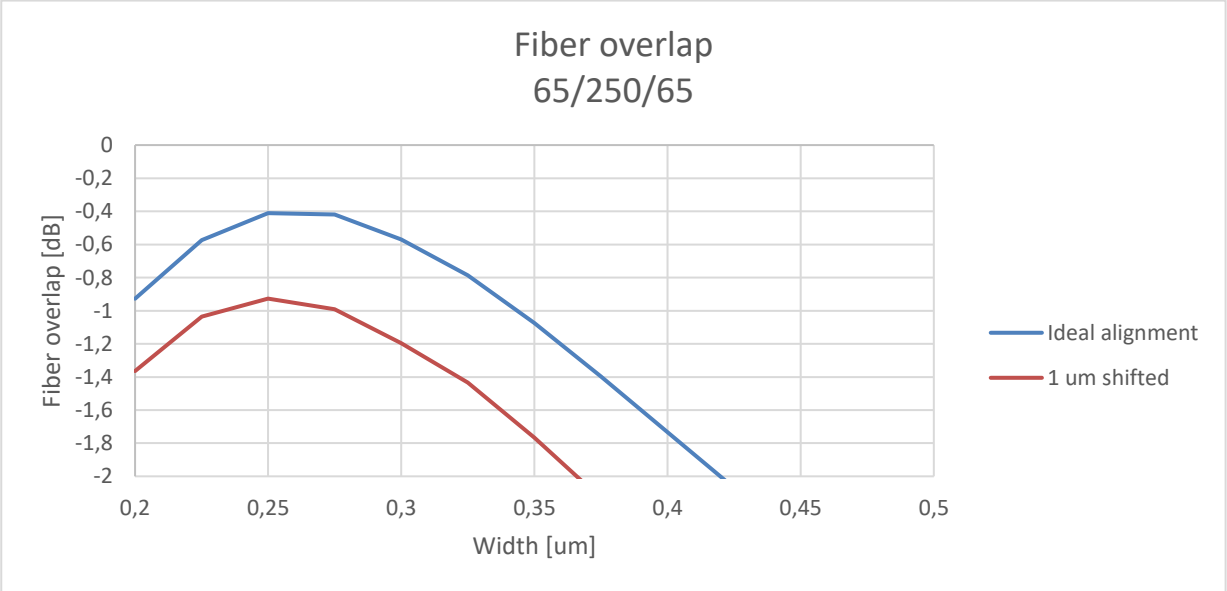

Figure 5: Losses for fiber-chip coupling based on the mode overlap. Ideal alignment shown inblue and 1µm shift from the centre shown in red.

As can be seen in Figure 5, an optimal coupling loss of -0.4dB can be achieved at ideal alignment with a waveguide width of 0.25 µm. At a misalignment of already 1µm this is reduced to -0.9 dB. It has to be noted that this mode profile was calculated with a co-called horizontal taper where one the SiN stripe is removed in the processing to allow for larger mode profiles and, hence, a better fiber-chip coupling. Based on the results of Figure 5, we chose to use a waveguide width of 0.25µm for the spot-size converters at the in- and output facets.

The last simulation that was performed for the waveguide cross-section was the thickness of the top cladding. The top cladding thickness must be chosen such that it gives low excess loss at the thermo-optic heaters while keeping them as close as possible to allow of efficient tuners to reduce thermal crosstalk.

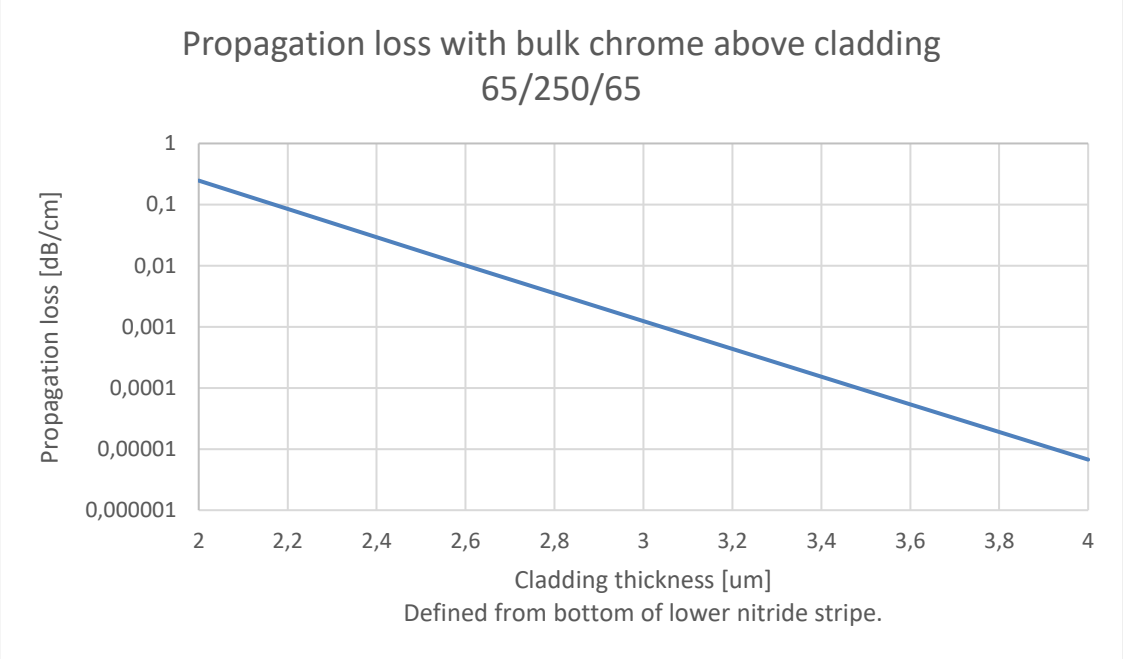

Figure 6: Excess loss induced by the material (chrome) of the thermo-optic heater as a function of top cladding thickness.

Based on the results shown in Figure 6, we chose to use a top cladding thickness of 3 µm as we consider an excess loss of 0.001 dB/cm low compared to the expected waveguide losses of 0.1-0.3 dB/cm at a wavelength of 925nm.

Conclusion

In this deliverable, we described the design consideration for the architecture of the silicon nitride platform. For the first generation of chips, we chose a tested architecture based on the QuiX decompositions. We calculated and designed the basic building blocks of the silicon nitride platform to optimize its performance for the targeted wavelength of 925nm of the quantum dot-based single photon sources.

By carefully designing the waveguide geometry, we found that a symmetric double stripe approach with a waveguide thickness of 65 nm and a width of 1.0 µm is expected to give the highest performance in terms of robust directional couplers and foot-print of the device.

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